Day : Wednesday

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Date: 5/30/2007
Time: 16:30:16

Inventor Name Search Result

Your Search was:

Last Name = CHOE
First Name = KWANG Su

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09998412	Not Issued	71	12/03/2001	Electronic commerce system and operating method thereof	CHOE, KWANG SOO
10334220	6800518	150	12/30/2002	FORMATION OF PATTERNED SILICON-ON-INSULATOR (SOI)/SILICON-ON-NOTHING (SON) COMPOSITE STRUCTURE BY POROUS SI ENGINEERING	CHOE, KWANG SU
10336147	6878611	150	01/02/2003	PATTERNED STRAINED SILICON FOR HIGH PERFORMANCE CIRCUITS	CHOE, KWANG SU
10662028	7125458	150	09/12/2003	FORMATION OF A SILICON GERMANIUM-ON-INSULATOR STRUCTURE BY OXIDATION OF A BURIED POROUS SILICON LAYER	CHOE, KWANG SU
10674647 this	Not Issued	30	09/30/2003	Thin buried oxides by low-dose oxygen implantation into modified silicon	CHOE, KWANG SU
10674648 copy	Not Issued	30	09/30/2003	SOI by oxidation of porous silicon	CHOE, KWANG SU

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Inventor Search Completed: No Records to Display.

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Date: 5/30/2007
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Inventor Name Search Result

Your Search was:

Last Name = MITCHELL
First Name = RYAN M.

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09805380	Not Issued	160	03/13/2001	Method and system for analyzing and planning an inventory	MITCHELL, RYAN J.
09805720	Not Issued	161	03/08/2001	Method and system for analyzing and planning an inventory	MITCHELL, RYAN J.
11038975	Not Issued	30	01/19/2005	Voice-over-internet protocol gateway	MITCHELL, RYAN J.
60654328	Not Issued	159	02/17/2005	VOIP to wireless gateway	MITCHELL, RYAN J.
11367938	Not Issued	25	03/03/2006	VOIP gateway network	MITCHELL, RYAN JAMES
10674647	Not Issued	30	09/30/2003	Thin buried oxides by low-dose oxygen implantation into modified silicon	MITCHELL, RYAN M.
10710737	7071103	150	07/30/2004	CHEMICAL TREATMENT TO RETARD DIFFUSION IN A SEMICONDUCTOR OVERLAYER	MITCHELL, RYAN M.
10710826	Not Issued	95	08/05/2004	METHOD OF FORMING STRAINED SILICON MATERIALS WITH IMPROVED THERMAL CONDUCTIVITY	MITCHELL, RYAN M.

Inventor Search Completed: No Records to Display.

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Date: 5/30/2007
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Inventor Name Search Result

Your Search was:

Last Name = MAURER
First Name = SIEGFRIED L.

Application#	Patent#	Status	Date Filed	Title	Inventor Name
06272175	4344358	150	06/10/1981	PROCESSING CHAMBER, IN PARTICULAR SMOKING CHAMBER	MAURER, SIEGFRIED
09526119	Not Issued	168	03/15/2000	Process and circuit arrangement for connecting a mobile radio telephone to a telecommunications network for fixed network telephones	MAURER, SIEGFRIED
09884670	Not Issued	161	06/19/2001	Divot reduction in SIMOX layers	MAURER, SIEGFRIED L.
10604145	Not Issued	168	06/27/2003	METHOD OF FORMING SILICON-ON-INSULATOR WAFERS HAVING PROCESS RESISTANT APPLICATIONS	MAURER, SIEGFRIED L.
10604146	Not Issued	71	06/27/2003	METHOD OF FORMING SILICON-ON-INSULATOR WAFERS HAVING PROCESS RESISTANT APPLICATIONS	MAURER, SIEGFRIED L.
10604149	Not Issued	168	06/27/2003	Method Of Forming Silicon-On-Insulator Wafers Having Process Resistant Applications	MAURER, SIEGFRIED L.
10674647	Not Issued	30	09/30/2003	Thin buried oxides by low-dose oxygen implantation into modified silicon	MAURER, SIEGFRIED L.
10768341	Not Issued	161	01/30/2004	High electrical quality buried oxide in simox	MAURER, SIEGFRIED L.
10200822	6784072	150	07/22/2002	CONTROL OF BURIED OXIDE IN SIMOX	MAURER, SIEGFRIED LUTZ
10896812	Not Issued	71	07/22/2004	Control of buried oxide in SIMOX	MAURER, SIEGFRIED LUTZ

Inventor Search Completed: No Records to Display.

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Day : Wednesday

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Date: 5/30/2007
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Inventor Name Search Result

Your Search was:

Last Name = SADANA
First Name = DEVENDRA K

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09205433	6177289	150	12/04/1998	LATERAL TRENCH OPTICAL DETECTORS	SADANA, DEVENDRA
09691700	Not Issued	161	10/18/2000	Lateral trench optical detectors	SADANA, DEVENDRA
11679308	Not Issued	30	02/27/2007	STRAINED SILICON MADE BY PRECIPITATING CARBON FROM Si(1-x-y)GexCy ALLOY	SADANA, DEVENDRA
60816050	Not Issued	20	06/23/2006	Buried channel MOSFET using III-V compound semiconductor substrates and high k gate dielectrics	SADANA, DEVENDRA
09031289	6087242	150	02/26/1998	METHOD TO IMPROVE COMMERCIAL BONDED SOI MATERIAL	SADANA, DEVENDRA KUMAR
08898760	Not Issued	161 abd	07/23/1997	METHOD AND STRUCTURE FOR LATERAL GETTERING OF SILICON-ON-INSULATOR SUBSTRATES	SADANA, DEVENDRA K
60046793	Not Issued	159	02/27/1997	METHOD TO IMPROVE COMMERCIAL BONDED SOI MATERIAL	SADANA, DEVENDRA K
09708337	6404014	150	11/08/2000	PLANAR AND DENSELY PATTERNED SILICON-ON-INSULATOR STRUCTURE	SADANA, DEVENDRA K.
09757317	6657261	150	01/09/2001	GROUND-PLANE DEVICE WITH BACK OXIDE TOPOGRAPHY	SADANA, DEVENDRA K.
09791273	6429488	150	02/22/2001	DENSELY PATTERNED SILICON-ON-INSULATOR (SOI) REGION ON A WAFER	SADANA, DEVENDRA K.
09810236	Not Issued	161	03/16/2001	Body contact in SOI devices by electrically weakening the oxide under the body	SADANA, DEVENDRA K.

09861590	6846727	150	05/21/2001	PATTERNED SOI BY OXYGEN IMPLANTATION AND ANNEALING	SADANA, DEVENDRA K.
09861593	6486037	150	05/21/2001	CONTROL OF BURIED OXIDE QUALITY IN LOW DOSE SIMOX	SADANA, DEVENDRA K.
09861594	6602757	150	05/21/2001	SELF-ADJUSTING THICKNESS UNIFORMITY IN SOI BY HIGH-TEMPERATURE OXIDATION OF SIMOX AND BONDED SOI	SADANA, DEVENDRA K.
09861596	6541356	150	05/21/2001	THE ULTIMATE SIMOX	SADANA, DEVENDRA K.
09874131	Not Issued	161	06/05/2001	Planar substrate with patterned silicon-on- insulator region and self-aligned trench	SADANA, DEVENDRA K.
09884670	Not Issued	161	06/19/2001	Divot reduction in SIMOX layers	SADANA, DEVENDRA K.
10055138	6805962	150	01/23/2002	METHOD OF CREATING HIGH-QUALITY RELAXED SIGE-ON-INSULATOR FOR STRAINED SI CMOS APPLICATIONS	SADANA, DEVENDRA K.
10055139	6495429	150	01/23/2002	CONTROLLING INTERNAL THERMAL OXIDATION AND ELIMINATING DEEP DIVOTS IN SIMOX BY CHLORINE-BASED ANNEALING	SADANA, DEVENDRA K.
10063994	6642090	150	06/03/2002	FIN FET DEVICES FROM BULK SEMICONDUCTOR AND METHOD FOR FORMING	SADANA, DEVENDRA K.
10080804	6593205	150	02/21/2002	PATTERNED SOI BY FORMATION AND ANNIHILATION OF BURIED OXIDE REGIONS DURING PROCESSING	SADANA, DEVENDRA K.
10119931	6812114	150	04/10/2002	PATTERNED SOI BY FORMATION AND ANNIHILATION OF BURIED OXIDE REGIONS DURING PROCESSING	SADANA, DEVENDRA K.
10122009	Not Issued	161	04/11/2002	Medium dose simox over a wide BOX thickness range by a multiple implant, multiple anneal process	SADANA, DEVENDRA K.

10128794	6743651	150	04/23/2002	METHOD OF FORMING A SIGE-ON-INSULATOR SUBSTRATE USING SEPARATION BY IMPLANTATION OF OXYGEN	SADANA, DEVENDRA K.
10185580	6756639	150	06/28/2002	CONTROL OF BURIED OXIDE QUALITY IN LOW DOSE SIMOX	SADANA, DEVENDRA K.
10196611	6841457	150	07/16/2002	USE OF HYDROGEN IMPLANTATION TO IMPROVE MATERIAL PROPERTIES OF SILICON-GERMANIUM-ON-INSULATOR MATERIAL MADE BY THERMAL DIFFUSION	SADANA, DEVENDRA K.
10280661	6835983	150	10/25/2002	SILICON-ON-INSULATOR (SOI) INTEGRATED CIRCUIT (IC) CHIP WITH THE SILICON LAYERS CONSISTING OF REGIONS OF DIFFERENT THICKNESS	SADANA, DEVENDRA K.
10300189	6946373	150	11/20/2002	RELAXED, LOW-DEFECT SGOI FOR STRAINED SI CMOS APPLICATIONS	SADANA, DEVENDRA K.
10318601	6717216	150	12/12/2002	FIELD EFFECT TRANSISTOR WITH STRESSED CHANNEL AND METHOD FOR MAKING SAME	SADANA, DEVENDRA K.
10334220	6800518	150	12/30/2002	FORMATION OF PATTERNED SILICON-ON-INSULATOR (SOI)/SILICON-ON-NOTHING (SON) COMPOSITE STRUCTURE BY POROUS SI ENGINEERING	SADANA, DEVENDRA K.
10336147	6878611	150	01/02/2003	PATTERNED STRAINED SILICON FOR HIGH PERFORMANCE CIRCUITS	SADANA, DEVENDRA K.
10341819	6717217	150	01/14/2003	ULTIMATE SIMOX	SADANA, DEVENDRA K.
10448947	6855436	150	05/30/2003	FORMATION OF SILICON-GERMANIUM-ON-INSULATOR (SGOI) BY AN INTEGRAL HIGH TEMPERATURE SIMOX-GE INTERDIFFUSION ANNEAL	SADANA, DEVENDRA K.

10448948	7049660	150	05/30/2003	HIGH-QUALITY SGOI BY OXIDATION NEAR THE ALLOY MELTING TEMPERATURE	SADANA, DEVENDRA K.
10448954	7026249	150	05/30/2003	SIGE LATTICE ENGINEERING USING A COMBINATION OF OXIDATION, THINNING AND EPITAXIAL REGROWTH	SADANA, DEVENDRA K.
10597066	Not Issued	25	07/10/2006	Method of forming thin sgoi wafers with high relaxation and low stacking fault defect density	SADANA, DEVENDRA K.
10604145	Not Issued	168	06/27/2003	METHOD OF FORMING SILICON-ON-INSULATOR WAFERS HAVING PROCESS RESISTANT APPLICATIONS	SADANA, DEVENDRA K.
10604146	Not Issued	71	06/27/2003	METHOD OF FORMING SILICON-ON-INSULATOR WAFERS HAVING PROCESS RESISTANT APPLICATIONS	SADANA, DEVENDRA K.
10604149	Not Issued	168	06/27/2003	Method Of Forming Silicon-On-Insulator Wafers Having Process Resistant Applications	SADANA, DEVENDRA K.
10604989	6875982	150	08/29/2003	AN ELECTRON MICROSCOPE MAGNIFICATION STANDARD PROVIDING PRECISE CALIBRATION IN THE MAGNIFICATION RANGE 5000X-2000,000X	SADANA, DEVENDRA K.
10610612	7169226	150	07/01/2003	DEFECT REDUCTION BY OXIDATION OF SILICON	SADANA, DEVENDRA K.
10654231	6803240	150	09/03/2003	METHOD OF MEASURING CRYSTAL DEFECTS IN THIN SI/SIGE BILAYERS	SADANA, DEVENDRA K.
10654232	6989058	150	09/03/2003	USE OF THIN SOI TO INHIBIT RELAXATION OF SIGE LAYERS	SADANA, DEVENDRA K.
10662028	7125458	150	09/12/2003	FORMATION OF A SILICON GERMANIUM-ON-INSULATOR STRUCTURE BY OXIDATION OF A BURIED POROUS SILICON LAYER	SADANA, DEVENDRA K.
10664714	6825102	150	09/18/2003	METHOD OF IMPROVING THE QUALITY OF DEFECTIVE SEMICONDUCTOR MATERIAL	SADANA, DEVENDRA K.

10669727	6884667	150	09/25/2003	FIELD EFFECT TRANSISTOR WITH STRESSED CHANNEL AND METHOD FOR MAKING SAME	SADANA, DEVENDRA K.
10674647	Not Issued	30	09/30/2003	Thin buried oxides by low-dose oxygen implantation into modified silicon	SADANA, DEVENDRA K.
10674648	Not Issued	30	09/30/2003	SOI by oxidation of porous silicon	SADANA, DEVENDRA K.
10685636	Not Issued	121	10/15/2003	Techniques for layer transfer processing	SADANA, DEVENDRA K.
10696601	6861158	150	10/29/2003	FORMATION OF SILICON-GERMANIUM-ON-INSULATOR (SGOI) BY AN INTEGRAL HIGH TEMPERATURE SIMOX-GE INTERDIFFUSION ANNEAL	SADANA, DEVENDRA K.

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Last Name = SADANA
First Name = DEVENDRA

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10700085	7084460	150	11/03/2003	METHOD FOR FABRICATING SIGE-ON-INSULATOR (SGOI) AND GE-ON-INSULATOR (GOI) SUBSTRATES	SADANA, DEVENDRA K.
10709114	6888221	150	04/14/2004	BICMOS TECHNOLOGY ON SIMOX WAFERS	SADANA, DEVENDRA K.
10710826	Not Issued	95	08/05/2004	METHOD OF FORMING STRAINED SILICON MATERIALS WITH IMPROVED THERMAL CONDUCTIVITY	SADANA, DEVENDRA K.
10725848	Not Issued	93	12/02/2003	ULTRA-THIN SI MOSFET DEVICE STRUCTURE AND METHOD OF MANUFACTURE	SADANA, DEVENDRA K.
10725849	7075150	150	12/02/2003	ULTRA-THIN SI CHANNEL MOSFET USING A SELF-ALIGNED OXYGEN IMPLANT AND DAMASCENE TECHNIQUE	SADANA, DEVENDRA K.
10751207	Not Issued	161	01/02/2004	Method of preventing surface roughening during hydrogen pre-bake of SiGe substrates using chlorine containing gases	SADANA, DEVENDRA K.
10751208	6958286	150	01/02/2004	METHOD OF PREVENTING SURFACE ROUGHENING DURING HYDROGEN PREBAKE OF SIGE SUBSTRATES	SADANA, DEVENDRA K.
10768341	Not Issued	161	01/30/2004	High electrical quality buried oxide in simox	SADANA, DEVENDRA K.
10818572	Not Issued	161	04/06/2004	Method of forming high-quality relaxed SiGe alloy layers on bulk Si substrates	SADANA, DEVENDRA K.

10824289	7074686	150	04/14/2004	METHOD OF CREATING HIGH-QUALITY RELAXED SIGE-ON-INSULATOR FOR STRAINED SI CMOS APPLICATIONS	SADANA, DEVENDRA K.
10830347	7087965	150	04/22/2004	STRAINED SILICON CMOS ON HYBRID CRYSTAL ORIENTATIONS	SADANA, DEVENDRA K.
10832215	6967376	150	04/26/2004	DIVOT REDUCTION IN SIMOX LAYERS	SADANA, DEVENDRA K.
10855915	Not Issued	61	05/27/2004	High-quality SGOI by annealing near the alloy melting point	SADANA, DEVENDRA K.
10883883	6991998	150	07/02/2004	ULTRA-THIN, HIGH QUALITY STRAINED SILICON-ON-INSULATOR FORMED BY ELASTIC STRAIN TRANSFER	SADANA, DEVENDRA K.
10883887	7172930	150	07/02/2004	STRAINED SILICON-ON-INSULATOR BY ANODIZATION OF A BURIED P+ SILICON GERMANIUM LAYER	SADANA, DEVENDRA K.
10890765	Not Issued	61	07/14/2004	Ion implantation for suppression of defects in annealed SiGe layers	SADANA, DEVENDRA K.
10900523	7067371	150	07/28/2004	SILICON-ON-INSULATOR (SOI) INTEGRATED CIRCUIT (IC) CHIP WITH THE SILICON LAYERS CONSISTING OF REGIONS OF DIFFERENT THICKNESS	SADANA, DEVENDRA K.
10902557	Not Issued	93	07/29/2004	DUAL SIMOX HYBRID ORIENTATION TECHNOLOGY (HOT) SUBSTRATES	SADANA, DEVENDRA K.
10905477	Not Issued	71	01/06/2005	METHOD OF CREATING A Ge-RICH CHANNEL LAYER FOR HIGH-PERFORMANCE CMOS CIRCUITS	SADANA, DEVENDRA K.
10905595	Not Issued	71	01/12/2005	LOW CONCENTRATION SiGe BUFFER DURING STRAINED Si GROWTH OF SSGOI MATERIAL FOR DOPANT DIFFUSION CONTROL AND DEFECT REDUCTION	SADANA, DEVENDRA K.
10923246	7115463	150	08/20/2004	PATTERNING SOI WITH SILICON MASK TO CREATE BOX AT DIFFERENT DEPTHS	SADANA, DEVENDRA K.

10932598	7141115	150	09/02/2004	METHOD OF PRODUCING SILICON-GERMANIUM-ON-INSULATOR MATERIAL USING UNSTRAINED GE-CONTAINING SOURCE LAYERS	SADANA, DEVENDRA K.
10982411	Not Issued	71	11/05/2004	Use of hydrogen implantation to improve material properties of silicon-germanium-on-insulator material made by thermal diffusion	SADANA, DEVENDRA K.
10984212	Not Issued	41	11/09/2004	Formation of silicon-germanium-on-insulator (SGOI) by an integral high temperature SIMOX-Ge interdiffusion anneal	SADANA, DEVENDRA K.
10992150	7141457	150	11/18/2004	METHOD TO FORM SI-CONTAINING SOI AND UNDERLYING SUBSTRATE WITH DIFFERENT ORIENTATIONS	SADANA, DEVENDRA K.
10993270	Not Issued	61	11/19/2004	Patterned SOI by oxygen implantation and annealing	SADANA, DEVENDRA K.
11029921	Not Issued	41	01/05/2005	High-quality SGOI by oxidation near the alloy melting temperature	SADANA, DEVENDRA K.
11031165	Not Issued	30	01/07/2005	Quasi-hydrophobic Si-Si wafer bonding using hydrophilic Si surfaces and dissolution of interfacial bonding oxide	SADANA, DEVENDRA K.
11039602	7084050	150	01/19/2005	FORMATION OF SILICON-GERMANIUM-ON-INSULATOR (SGOI) BY AN INTEGRAL HIGH TEMPERATURE SIMOX-GE INTERDIFFUSION ANNEAL	SADANA, DEVENDRA K.
11116053	Not Issued	30	04/27/2005	Field effect transistor with mixed-crystal-orientation channel and source/drain regions	SADANA, DEVENDRA K.
11164345	Not Issued	30	11/18/2005	HYBRID CRYSTALLOGRAPHIC SURFACE ORIENTATION SUBSTRATE HAVING ONE OR MORE SOI REGIONS AND/OR BULK SEMICONDUCTOR REGIONS	SADANA, DEVENDRA K.
11208359	Not Issued	71	08/19/2005	Relaxed, low-defect SGOI for strained Si CMOS applications	SADANA, DEVENDRA K.

11259654	Not Issued	71	10/26/2005	Method for tuning epitaxial growth by interfacial doping and structure including same	SADANA, DEVENDRA K.
11268096	Not Issued	71	11/07/2005	Use of thin SOI to inhibit relaxation of SiGe layers	SADANA, DEVENDRA K.
11293774	Not Issued	30	12/02/2005	Ultra-thin, high quality strained silicon-on-insulator formed by elastic strain transfer	SADANA, DEVENDRA K.
11327675	Not Issued	25	01/06/2006	High k gate stack on III-V compound semiconductors	SADANA, DEVENDRA K.
11332564	Not Issued	71	01/13/2006	Strained semiconductor-on-insulator (sSOI) by a simox method	SADANA, DEVENDRA K.
11333074	Not Issued	30	01/17/2006	Structure and method to form semiconductor-on-pores (SOP) for high device performance and low manufacturing cost	SADANA, DEVENDRA K.
11384718	Not Issued	30	03/15/2006	Structure and method for controlling the behavior of dislocations in strained semiconductor layers	SADANA, DEVENDRA K.
11401672	Not Issued	30	04/11/2006	CMOS process with Si gates for nFETs and SiGe gates for pFETs	SADANA, DEVENDRA K.
11402177	Not Issued	30	04/11/2006	Control of poly-Si depletion in CMOS via gas phase doping	SADANA, DEVENDRA K.
11417846	Not Issued	30	05/04/2006	Ion implantation combined with in situ or ex situ heat treatment for improved field effect transistors	SADANA, DEVENDRA K.
11436756	Not Issued	30	05/18/2006	Ultra-thin Si channel MOSFET using a self-aligned oxygen implant and damascene technique	SADANA, DEVENDRA K.
11481525	Not Issued	41	07/06/2006	Method for fabricating SiGe-on-insulator (SGOI) and Ge-on-insulator (GOI) substrates	SADANA, DEVENDRA K.
11492271	Not Issued	30	07/25/2006	Strained silicon CMOS on hybrid crystal orientations	SADANA, DEVENDRA K.
11619040	Not Issued	30	01/02/2007	DEFECT REDUCTION BY OXIDATION OF SILICON	SADANA, DEVENDRA K.
11620224	Not Issued	25	01/05/2007	Structures containing electrodeposited germanium and methods for their fabrication	SADANA, DEVENDRA K.
11620663	Not Issued	30	01/06/2007	STRAINED SILICON-ON-INSULATOR BY ANODIZATION OF A BURIED p+ SILICON GERMANIUM	SADANA, DEVENDRA K.

				LAYER	
11678338	Not Issued	25	02/23/2007	LOW-TEMPERATURE ELECTRICALLY ACTIVATED GATE ELECTRODE AND METHOD OF FABRICATING SAME	SADANA, DEVENDRA K.
06210488	4371774	150	11/26/1980	HIGH POWER LINEAR PULSED BEAM ANNEALER	SADANA, DEVENDRA K.

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Last Name = SADANA
First Name = DEVENDRA

Application#	Patent#	Status	Date Filed	Title	Inventor Name
07487501	Not Issued	166	03/02/1990	CONTROLLED SILICON DOPING OF III-V COMPOUNDS BY THERMAL OXIDATION OF SILICON CAPPING LAYER	SADANA, DEVENDRA K.
07655512	5183767	250	02/14/1991	METHOD FOR INTERNAL GETTERING OF OXYGEN IN III-V COMPOUND SEMICONDUCTORS	SADANA, DEVENDRA K.
07754276	5188978	250	08/30/1991	CONTROLLED SILICON DOPING OF III-V COMPOUNDS BY THERMAL OXIDATION OF SILICON CAPPING LAYER	SADANA, DEVENDRA K.
07913560	5242859	250	07/14/1992	HIGHLY DOPED SEMICONDUCTOR MATERIAL AND METHOD OF FABRICATION THEREOF	SADANA, DEVENDRA K.
07945858	5272373	250	09/16/1992	INTERNAL GETTERING OF OXYGEN IN III-V COMPOUND SEMICONDUCTORS	SADANA, DEVENDRA K.
08575421	Not Issued	161	12/20/1995	METHOD AND STRUCTURE FOR LATERAL GETTERING OF SILICON-ON-INSULATOR SUBSTRATES	SADANA, DEVENDRA K.
08678442	5767549	150	07/03/1996	SOI CMOS STRUCTURE	SADANA, DEVENDRA K.
09193606	6214694	150	11/17/1998	PROCESS OF MAKING DENSELY PATTERNED SILICON-ON-INSULATOR (SOI) REGION ON A WAFER	SADANA, DEVENDRA K.
09227696	6255145	150	01/08/1999	PROCESS FOR MANUFACTURING PATTERNED SILICON-ON-	SADANA, DEVENDRA K.

				INSULATOR LAYERS WITH SELF- ALIGNED TRENCHES AND RESULTING PRODUCT	
09250895	6180486	150	02/16/1999	PROCESS OF FABRICATING PLANAR AND DENSELY PATTERNED SILICON-ON-INSULATOR STRUCTURE	SADANA, DEVENDRA K.
09427256	6426252	150	10/25/1999	SILICON-ON-INSULATOR VERTICAL ARRAY DRAM CELL WITH SELF-ALIGNED BURIED STRAP	SADANA, DEVENDRA K.
09427257	6566177	150	10/25/1999	SILICON-ON-INSULATOR VERTICAL ARRAY DEVICE TRENCH CAPACITOR DRAM	SADANA, DEVENDRA K.
60032331	Not Issued	159	12/03/1996	SILICON-ON-INSULATOR SUBSTRATES USING LOW DOSE IMPLANTATION	SADANA, DEVENDRA K.
60039989	Not Issued	159	03/05/1997	METHOD OF FORMING BURIED OXIDE LAYERS IN SILICON	SADANA, DEVENDRA K.
09531628	6222253	150	03/21/2000	Buried Oxide Layer In Silicon	SADANA, DEVENDRA KUMAR
09567095	6300218	150	05/08/2000	Method for patterning a buried oxide thickness for a separation by implanted oxygen (simox) process	SADANA, DEVENDRA KUMAR
09788979	6432754	150	02/20/2001	DOUBLE SOI DEVICE WITH RECESS ETCH AND EPITAXY	SADANA, DEVENDRA KUMAR
09975435	6756257	150	10/11/2001	PATTERNED SOI REGIONS ON SEMICONDUCTOR CHIPS	SADANA, DEVENDRA KUMAR
10200822	6784072	150	07/22/2002	CONTROL OF BURIED OXIDE IN SIMOX	SADANA, DEVENDRA KUMAR
10896812	Not Issued	71	07/22/2004	Control of buried oxide in SIMOX	SADANA, DEVENDRA KUMAR
10990300	Not Issued	41	11/15/2004	Ultrathin buried insulators in Si or Si-containing material	SADANA, DEVENDRA KUMAR
11031142	Not Issued	41	01/07/2005	Method for fabricating low-defect-density changed orientation Si	SADANA, DEVENDRA KUMAR

11046912	Not Issued	93	01/31/2005	STRUCTURE AND METHOD OF INTEGRATING COMPOUND AND ELEMENTAL SEMICONDUCTORS FOR HIGH-PERFORMACE CMOS	SADANA, DEVENDRA KUMAR
08961131	6043166	150	10/30/1997	SILICON-ON-INSULATOR SUBSTRATES USING LOW DOSE IMPLANTATION	SADANA, DEVENDRA KUMAR
08995585	5930643	150	12/22/1997	DEFECT INDUCED BURIED OXIDE (DIBOX) FOR THROUGHPUT SOI	SADANA, DEVENDRA KUMAR
09034445	6090689	150	03/04/1998	METHOD OF FORMING BURIED OXIDE LAYERS IN SILICON	SADANA, DEVENDRA KUMAR
09264973	6259137	150	03/09/1999	DEFECT INDUCED BURIED OXIDE (DIBOX) FOR THROUGHPUT SOI	SADANA, DEVENDRA KUMAR
09312217	6204546	150	05/14/1999	SILICON-ON-INSULATOR SUBSTRATES USING LOW DOSE IMPLANTATION	SADANA, DEVENDRA KUMAR
09356295	6333532	150	07/16/1999	PATTERNED SOI REGIONS IN SEMICONDUCTOR CHIPS	SADANA, DEVENDRA KUMAR

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Your Search was:

Last Name = FOGEL
First Name = KEITH E.

Application#	Patent#	Status	Date Filed	Title	Inventor Name
07485016	4975079	250	02/23/1990	CONNECTOR ASSEMBLY FOR CHIP TESTING	FOGEL, KEITH
10710826	Not Issued	95	08/05/2004	METHOD OF FORMING STRAINED SILICON MATERIALS WITH IMPROVED THERMAL CONDUCTIVITY	FOGEL, KEITH
10928473	7172431	150	08/27/2004	ELECTRICAL CONNECTOR DESIGN AND CONTACT GEOMETRY AND METHOD OF USE THEREOF AND METHODS OF FABRICATION THEREOF	FOGEL, KEITH
09081342	6525551	150	05/19/1998	PROBE STRUCTURES FOR TESTING ELECTRICAL INTERCONNECTIONS TO INTEGRATED CIRCUIT ELECTRONIC DEVICES	FOGEL, KEITH EDWARD
10336147	6878611	150	01/02/2003	PATTERNED STRAINED SILICON FOR HIGH PERFORMANCE CIRCUITS	FOGEL, KEITH E
60026088	Not Issued	159	09/13/1996	WAFER SCALE HIGH DENSITY PROBE ASSEMBLY	FOGEL, KEITH E
09861590	6846727	150	05/21/2001	PATTERNED SOI BY OXYGEN IMPLANTATION AND ANNEALING	FOGEL, KEITH E.
09861596	6541356	150	05/21/2001	THE ULTIMATE SIMOX	FOGEL, KEITH E.
10055138	6805962	150	01/23/2002	METHOD OF CREATING HIGH-QUALITY RELAXED SIGE-ON-INSULATOR FOR STRAINED SI CMOS APPLICATIONS	FOGEL, KEITH E.
10196611	6841457	150	07/16/2002	USE OF HYDROGEN IMPLANTATION TO IMPROVE MATERIAL PROPERTIES OF	FOGEL, KEITH E.

				SILICON-GERMANIUM-ON-INSULATOR MATERIAL MADE BY THERMAL DIFFUSION	
10300189	6946373	150	11/20/2002	RELAXED, LOW-DEFECT SGOI FOR STRAINED SI CMOS APPLICATIONS	FOGEL, KEITH E.
10334220	6800518	150	12/30/2002	FORMATION OF PATTERNED SILICON-ON-INSULATOR (SOI)/SILICON-ON-NOTHING (SON) COMPOSITE STRUCTURE BY POROUS SI ENGINEERING	FOGEL, KEITH E.
10341819	6717217	150	01/14/2003	ULTIMATE SIMOX	FOGEL, KEITH E.
10448947	6855436	150	05/30/2003	FORMATION OF SILICON-GERMANIUM-ON-INSULATOR (SGOI) BY AN INTEGRAL HIGH TEMPERATURE SIMOX-GE INTERDIFFUSION ANNEAL	FOGEL, KEITH E.
10448948	7049660	150	05/30/2003	HIGH-QUALITY SGOI BY OXIDATION NEAR THE ALLOY MELTING TEMPERATURE	FOGEL, KEITH E.
10448954	7026249	150	05/30/2003	SIGE LATTICE ENGINEERING USING A COMBINATION OF OXIDATION, THINNING AND EPITAXIAL REGROWTH	FOGEL, KEITH E.
10531494	Not Issued	30	04/15/2005	Land grid array fabrication using elastomer core and conducting metal shell or mesh	FOGEL, KEITH E.
10610612	7169226	150	07/01/2003	DEFECT REDUCTION BY OXIDATION OF SILICON	FOGEL, KEITH E.
10654231	6803240	150	09/03/2003	METHOD OF MEASURING CRYSTAL DEFECTS IN THIN SI/SIGE BILAYERS	FOGEL, KEITH E.
10654232	6989058	150	09/03/2003	USE OF THIN SOI TO INHIBIT RELAXATION OF SIGE LAYERS	FOGEL, KEITH E.
10662028	7125458	150	09/12/2003	FORMATION OF A SILICON GERMANIUM-ON-INSULATOR STRUCTURE BY OXIDATION OF A BURIED POROUS SILICON LAYER	FOGEL, KEITH E.
10664714	6825102	150	09/18/2003	METHOD OF IMPROVING THE QUALITY OF DEFECTIVE SEMICONDUCTOR MATERIAL	FOGEL, KEITH E.

10674647	Not Issued	30	09/30/2003	Thin buried oxides by low-dose oxygen implantation into modified silicon	FOGEL, KEITH E.
10674648	Not Issued	30	09/30/2003	SOI by oxidation of porous silicon	FOGEL, KEITH E.
10696601	6861158	150	10/29/2003	FORMATION OF SILICON-GERMANIUM-ON-INSULATOR (SGOI) BY AN INTEGRAL HIGH TEMPERATURE SIMOX-GE INTERDIFFUSION ANNEAL	FOGEL, KEITH E.
10715288	7137827	150	11/17/2003	INTERPOSER WITH ELECTRICAL CONTACT BUTTON AND METHOD	FOGEL, KEITH E.
10768341	Not Issued	161	01/30/2004	High electrical quality buried oxide in simox	FOGEL, KEITH E.
10815103	Not Issued	41	03/31/2004	Interconnections for flip-chip using lead-free solders and having reaction barrier layers	FOGEL, KEITH E.
10818572	Not Issued	161	04/06/2004	Method of forming high-quality relaxed SiGe alloy layers on bulk Si substrates	FOGEL, KEITH E.
10824289	7074686	150	04/14/2004	METHOD OF CREATING HIGH-QUALITY RELAXED SIGE-ON-INSULATOR FOR STRAINED SI CMOS APPLICATIONS	FOGEL, KEITH E.
10855915	Not Issued	61	05/27/2004	High-quality SGOI by annealing near the alloy melting point	FOGEL, KEITH E.
10883883	6991998	150	07/02/2004	ULTRA-THIN, HIGH QUALITY STRAINED SILICON-ON-INSULATOR FORMED BY ELASTIC STRAIN TRANSFER	FOGEL, KEITH E.
10883887	7172930	150	07/02/2004	STRAINED SILICON-ON-INSULATOR BY ANODIZATION OF A BURIED P+ SILICON GERMANIUM LAYER	FOGEL, KEITH E.
10890765	Not Issued	61	07/14/2004	Ion implantation for suppression of defects in annealed SiGe layers	FOGEL, KEITH E.
10932598	7141115	150	09/02/2004	METHOD OF PRODUCING SILICON-GERMANIUM-ON-INSULATOR MATERIAL USING UNSTRAINED GE-CONTAINING SOURCE LAYERS	FOGEL, KEITH E.

10982411	Not Issued	71	11/05/2004	Use of hydrogen implantation to improve material properties of silicon-germanium-on-insulator material made by thermal diffusion	FOGEL, KEITH E.
10984212	Not Issued	41	11/09/2004	Formation of silicon-germanium-on-insulator (SGOI) by an integral high temperature SIMOX-Ge interdiffusion anneal	FOGEL, KEITH E.
10993270	Not Issued	61	11/19/2004	Patterned SOI by oxygen implantation and annealing	FOGEL, KEITH E.
11029921	Not Issued	41	01/05/2005	High-quality SGOI by oxidation near the alloy melting temperature	FOGEL, KEITH E.
11039602	7084050	150	01/19/2005	FORMATION OF SILICON-GERMANIUM-ON-INSULATOR (SGOI) BY AN INTEGRAL HIGH TEMPERATURE SIMOX-GE INTERDIFFUSION ANNEAL	FOGEL, KEITH E.
11208359	Not Issued	71	08/19/2005	Relaxed, low-defect SGOI for strained Si CMOS applications	FOGEL, KEITH E.
11220324	Not Issued	30	09/06/2005	Interposer with electrical contact button and method	FOGEL, KEITH E.
11268096	Not Issued	71	11/07/2005	Use of thin SOI to inhibit relaxation of SiGe layers	FOGEL, KEITH E.
11293774	Not Issued	30	12/02/2005	Ultra-thin, high quality strained silicon-on-insulator formed by elastic strain transfer	FOGEL, KEITH E.
11332564	Not Issued	71	01/13/2006	Strained semiconductor-on-insulator (sSOI) by a simox method	FOGEL, KEITH E.
11333074	Not Issued	30	01/17/2006	Structure and method to form semiconductor-on-pores (SOP) for high device performance and low manufacturing cost	FOGEL, KEITH E.
11406122	Not Issued	30	04/18/2006	Laser processing method for trench-edge-defect-free solid phase epitaxy in confined geometrics	FOGEL, KEITH E.
11424642	Not Issued	30	06/16/2006	THERMALLY CONDUCTIVE COMPOSITE INTERFACE, COOLED ELECTRONIC ASSEMBLIES EMPLOYING THE SAME, AND METHODS OF FABRICATION THEREOF	FOGEL, KEITH E.
11561273	Not Issued	25	11/17/2006	INTERPOSER WITH ELECTRICAL CONTACT BUTTON AND METHOD	FOGEL, KEITH E.

11619040	Not Issued	30	01/02/2007	DEFECT REDUCTION BY OXIDATION OF SILICON	FOGEL, KEITH E.

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Application#	Patent#	Status	Date Filed	Title	Inventor Name
11620663	Not Issued	30	01/06/2007	STRAINED SILICON-ON-INSULATOR BY ANODIZATION OF A BURIED p+ SILICON GERMANIUM LAYER	FOGEL, KEITH E.
11678338	Not Issued	25	02/23/2007	LOW-TEMPERATURE ELECTRICALLY ACTIVATED GATE ELECTRODE AND METHOD OF FABRICATING SAME	FOGEL, KEITH E.
60421480	Not Issued	159	10/24/2002	Land grid array fabrication using elastomer core and conducting metal shell or mesh	FOGEL, KEITH E.
07963346	5371654	150	10/19/1992	THREE DIMENSIONAL HIGH PERFORMANCE INTERCONNECTION PACKAGE	FOGEL, KEITH E.
08055485	5635846	150	04/30/1993	TEST PROBE HAVING ELONGATED CONDUCTOR EMBEDDED IN AN ELASTOMERIC MATERIAL WHICH IS MOUNTED ON A SPACE TRANSFORMER	FOGEL, KEITH E.
08224383	Not Issued	166	04/07/1994	INTEGRAL RIGID CHIP TEST PROBE	FOGEL, KEITH E.
08300620	5531022	150	09/02/1994	METHOD OF FORMING A THREE DIMENSIONAL HIGH PERFORMANCE INTERCONNECTION PACKAGE	FOGEL, KEITH E.
08323554	5541567	150	10/17/1994	COAXIAL VIAS IN AN ELECTRONIC SUBSTRATE	FOGEL, KEITH E.
08324053	Not Issued	161	10/17/1994	METHODS OF FABRICATION OF COAXIAL VIAS AND	FOGEL, KEITH E.

				MAGNETIC DEVICES	
08425543	Not Issued	161	04/20/1995	HIGH DENSITY INTEGRAL TEST PROBE AND FABRICATION METHOD	FOGEL, KEITH E.
08425639	Not Issued	161	04/20/1995	HIGH TEMPERATURE CHIP TEST PROBE	FOGEL, KEITH E.
08527733	5810607	150	09/13/1995	INTERCONNECTOR WITH CONTACT PADS HAVING ENHANCED DURABILITY	FOGEL, KEITH E.
08614417	5811982	150	03/12/1996	HIGH DENSITY CANTILEVERED PROBE FOR ELECTRONIC DEVICES	FOGEL, KEITH E.
08614456	Not Issued	160	03/12/1996	HIGH DENSITY TEST PROBE WITH RIGID SURFACE STRUCTURE	FOGEL, KEITH E.
08641667	5785538	150	05/01/1996	HIGH DENSITY TEST PROBE WITH RIGID SURFACE STRUCTURE	FOGEL, KEITH E.
08739343	6286208	150	10/28/1996	INTERCONNECTOR WITH CONTACT PADS HAVING ENHANCED DURABILITY	FOGEL, KEITH E.
08744903	5838160	150	11/08/1996	INTEGRAL RIGID CHIP TEST PROBE	FOGEL, KEITH E.
08752469	6054651	150	11/19/1996	FOAMED ELASTOMERS FOR WAFER PROBING APPLICATIONS AND INTERPOSER CONNECTORS	FOGEL, KEITH E.
08754869	5821763	150	11/22/1996	TEST PROBE FOR HIGH DENSITY INTEGRATED CIRCUITS METHODS OF FABRICATION THEREOF AND METHODS OF USE THEREOF	FOGEL, KEITH E.
08756830	Not Issued	167	11/20/1996	HIGH DENSITY INTEGRAL TEST PROBE	FOGEL, KEITH E.
08756831	Not Issued	161	11/20/1996	HIGH TEMPERATURE CHIP TEST PROBE	FOGEL, KEITH E.
09076267	6078500	150	05/12/1998	PLUGGABLE CHIP SCALE PACKAGE	FOGEL, KEITH E.
09162717	Not Issued	169	09/29/1998	PLATED PROBE STRUCTURE	FOGEL, KEITH E.
09164470	6295729	150	10/01/1998	ANGLED FLYING LEAD WIRE BONDING PROCESS	FOGEL, KEITH E.
09251988	Not Issued	41	02/17/1999	STRUCTURAL DESIGN AND PROCESSES TO CONTROL PROBE POSITION ACCURACY	FOGEL, KEITH E.

				IN A WAFER TEST PROBE ASSEMBLY	
60020000	Not Issued	159	06/21/1996	FOAMED ELASTOMERS FOR WAFER PROBING APPLICATIONS AND INTERPOSER CONNECTORS	FOGEL, KEITH E.
60026050	Not Issued	159	09/13/1996	CHIP PROBE STRUCTURE HAVING A PLURALITY OF DISCRETE INSULATED PROBE TIPS PROJECTING FROM A SUPPORT SURFACE	FOGEL, KEITH E.
60026112	Not Issued	159	09/13/1996	INTEGRATED COMPLIANT PROBE FOR WAFER LEVEL TEST AND BURNIN	FOGEL, KEITH E.
60047556	Not Issued	159	05/22/1997	PROBE STRUCTURE WITH ENHANCED DURABILITY	FOGEL, KEITH E.
60047558	Not Issued	159	05/22/1997	PLUGGABLE CHIP SCALE PACKAGE	FOGEL, KEITH E.
60060877	Not Issued	159	10/02/1997	ANGLED FLYING LEAD WIRE BONDING PROCESS	FOGEL, KEITH E.
60060878	Not Issued	159	10/02/1997	PLATED PROBE STRUCTURE	FOGEL, KEITH E.
09165832	6891360	150	10/02/1998	PLATED PROBE STRUCTURE	FOGEL, KEITH EDWARD
09254768	6528984	150	03/11/1999	INTEGRATED COMPLIANT PROBE FOR WAFER LEVEL TEST AND BURN-IN	FOGEL, KEITH EDWARD
09834848	Not Issued	161	04/13/2001	Deformable coated wick liquid spilled material transfer	FOGEL, KEITH EDWARD
09871536	6526655	150	05/31/2001	ANGLED FLYING LEAD WIRE BONDING PROCESS	FOGEL, KEITH EDWARD
09886960	6523255	150	06/21/2001	PROCESS AND STRUCTURE TO REPAIR DAMAGED PROBES MOUNTED ON A SPACE TRANSFORMER	FOGEL, KEITH EDWARD
09921867	Not Issued	61	08/03/2001	High density integrated circuit apparatus, test probe and methods of use thereof	FOGEL, KEITH EDWARD
09928285	6722032	150	08/10/2001	A METHOD OF FORMING A STURCTURE FOR ELECTRONIC DEVICES CONTACT LOCATIONS	FOGEL, KEITH EDWARD
09972622	Not Issued	161	10/09/2001	HIGH DENSITY INTEGRAL TEST PROBE APPARATUS FOR TESTING ELECTRONIC	FOGEL, KEITH EDWARD

				DEVICES	
10066171	Not Issued	41	02/01/2002	Probe structure having a plurality of discrete insulated probe tips projecting from a support surface, apparatus for use thereof and methods of fabrication thereof	FOGEL, KEITH EDWARD
10145661	Not Issued	71	05/14/2002	STRUCTURAL DESIGN AND PROCESSES TO CONTROL PROBE POSITION ACCURACY IN A WAFER TEST PROBE ASSEMBLY	FOGEL, KEITH EDWARD
10202069	Not Issued	41	07/23/2002	Probe structure having a plurality of discrete insulated probe tips projecting from a support surface, apparatus for use thereof and methods of fabrication thereof	FOGEL, KEITH EDWARD
10341794	Not Issued	161	01/14/2003	Compliant interposer assembly for wafer test and "burn-in" operations	FOGEL, KEITH EDWARD
10342167	6708403	150	01/14/2003	ANGLED FLYING LEAD WIRE BONDING PROCESS	FOGEL, KEITH EDWARD
10408200	Not Issued	41	04/04/2003	High density integrated circuit apparatus, test probe and methods of use thereof	FOGEL, KEITH EDWARD
10685636	Not Issued	121	10/15/2003	Techniques for layer transfer processing	FOGEL, KEITH EDWARD
10736890	Not Issued	41	12/16/2003	Angled flying lead wire bonding process	FOGEL, KEITH EDWARD
10742685	6880245	150	12/19/2003	A METHOD FOR FABRICATING A STRUCTURE FOR MAKING CONTACT WITH AN IC DEVICE	FOGEL, KEITH EDWARD
11031142	Not Issued	41	01/07/2005	Method for fabricating low-defect-density changed orientation Si	FOGEL, KEITH EDWARD

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Application#	Patent#	Status	Date Filed	Title	Inventor Name
11101309	Not Issued	71	04/07/2005	A METHOD FOR FABRICATING A STRUCTURE FOR MAKING CONTACT WITH A DEVICE	FOGEL, KEITH EDWARD
11142646	Not Issued	71	06/01/2005	Amorphization/templated recrystallization method for hybrid orientation substrates	FOGEL, KEITH EDWARD
08783738	5898991	150	01/16/1997	METHODS OF FABRICATION OF COAXIAL VIAS AND MAGNETIC DEVICES	FOGEL, KEITH EDWARD
08872519	6334247	150	06/11/1997	HIGH DENSITY INTEGRATED CIRCUIT APPARATUS, TEST PROBE AND METHODS OF USE THEREOF	FOGEL, KEITH EDWARD
08946141	5914614	150	10/07/1997	HIGH DENSITY CANTILEVERED PROBE FOR ELECTRONIC DEVICES	FOGEL, KEITH EDWARD
09078174	6062879	150	05/13/1998	HIGH DENSITY TEST PROBE WITH RIGID SURFACE STRUCTURE	FOGEL, KEITH EDWARD
09088394	6300780	150	06/01/1998	HIGH DENSITY INTEGRATED CIRCUIT APPARATUS, TEST PROBE AND METHODS OF USE THEREOF	FOGEL, KEITH EDWARD
09162474	6104201	150	09/28/1998	METHOD AND APPARATUS FOR PASSIVE CHARACTERIZATION OF SEMICONDUCTOR SUBSTRATES SUBJECTED TO HIGH ENERGY (MEV) ION IMPLEMENTATION USING HIGH-INJECTION SURFACE PHOTOVOLTAGE	FOGEL, KEITH EDWARD
09198179	6332270	150	11/23/1998	METHOD OF MAKING A HIGH DENSITY INTEGRAL TEST	FOGEL, KEITH EDWARD

				PROBE	
09208529	6329827	150	12/09/1998	HIGH DENSITY CANTILEVERED PROBE FOR ELECTRONIC DEVICES	FOGEL, KEITH EDWARD
09251864	6206273	150	02/17/1999	STRUCTURES AND PROCESSES TO CREATE A DESIRED PROBETIP CONTACT GEOMETRY ON A WAFER TEST PROBE	FOGEL, KEITH EDWARD
09254769	Not Issued	98	03/11/1999	WAFER SCALE HIGH DENSITY PROBE ASSEMBLY, APPARATUS FOR USE THEREOF AND METHODS OF FABRICATION THEREOF	FOGEL, KEITH EDWARD
09254798	6452406	150	03/11/1999	PROBE STRUCTURE HAVING A PLURALITY OF DISCRETE INSULATED PROBE TIPS	FOGEL, KEITH EDWARD
09382834	Not Issued	40	08/25/1999	HIGH DENSITY INTEGRATED CIRCUIT APPARATUS, TEST PROBE AND METHODS OF USE THEREOF	FOGEL, KEITH EDWARD

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Inventor Information for 10/674647

Inventor Name	City	State/Country
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MAURER, SIEGFRIED L.	STORMVILLE	NEW YORK
MITCHELL, RYAN M.	CLINTONDALE	NEW YORK
SADANA, DEVENDRA K.	PLEASANTVILLE	NEW YORK

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